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TO: EXAMINER: HENRY TSAI (ART UNIT 2183)

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FROM: PAUL J. DITMYER, ESQ.

DATE: August 23, 2005

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COMMENTS/INSTRUCTIONS:

Please see attached Appellant's Appeal Brief for U.S. Patent Application Serial No. 10/082,816.

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS**

In re Patent Application of: **COFLER ET AL.**	Examiner: **Henry TSAI**
Serial No. **10/082,816** Confirmation No. **1555** Filing Date: **FEBRUARY 25, 2002**	Art Unit: **2183**
For: **METHOD OF HANDLING BRANCHING INSTRUCTIONS WITHIN A PROCESSOR, IN PARTICULAR A PROCESSOR FOR DIGITAL SIGNAL PROCESSING, AND CORRESPONDING PROCESSOR**	

APPELLANT'S APPEAL BRIEF

MS Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellant's Appeal Brief together with the requisite $500.00 large entity fee for filing a brief. If any additional extension and/or fee is required, authorization is given to charge Deposit Account No. **01-0484.**

(1) Real Party in Interest

The real party in interest is STMicroelectronics SA, assignee of the present application as recorded at Reel 12848, Frame 882.

(2) Related Appeals and Interferences

At present there are no related appeals or interferences.

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(3) Status of the Claims

Claims 25-50 are pending in the application, of which Claims 25-27, 30, 36-40 and 50 are being appealed herein.

(4) Status of the Amendments

All amendments have been entered and there are no further pending amendments. A copy of the claims involved in this appeal is attached hereto as Appendix A.

(5) Summary of the Claimed Subject Matter

In general, the present invention is directed to a mechanism for handling branching instructions that allows an overall improvement in the branching latency, and applies particularly to a processor including decoupled architecture. According to the invention, with the processor core being clocked by a clock signal, a branching instruction received by the central unit in the course of a current cycle of the clock signal is processed in the course of the current cycle. The branching module is in the central unit, which makes it possible to process the branching instructions much more rapidly.

Referring to FIGs. 1 and 2 (FIG. 2 of which is reproduced below), and pages 14-15 of the specification, for example, the presently claimed invention (as set forth in independent Claims 25, 36 and 38) will now be described.

Independent Claim 25 is directed to a method of handling branching instructions using a processor PROC comprising a program memory PM storing program instructions, and a processor core CR comprising a plurality of processing units DU, AU and a central unit CU connected thereto, the central unit issuing instructions to the processing units based upon the program

instructions. The method includes clocking the processor core with a clock signal, receiving a branching instruction in the course of a current cycle, and processing the received branching instruction in the course of the current cycle.

Independent Claim 36 is directed to a method of handling branching instructions using a processor PROC comprising a program memory PM storing program instructions, and a processor core CR comprising a plurality of processing units DU, AU and a central unit CU connected thereto, the central unit issuing instructions to the processing units based upon the program instructions, the method including receiving at the central core a branching instruction during a current clock cycle and processing the received branching instruction during the current clock cycle.

Independent Claim 38 is directed to a processor PROC comprising a program memory PM for storing program instructions and a processor core CR being clocked by a clock signal and comprising a plurality of processing units DU, AU and a central unit CU connected thereto. The central unit is for issuing instructions to the processing units based upon corresponding program instructions. The central unit includes a branching module BRU for receiving a branching instruction during a current clock cycle, and processing this branching instruction during the current clock cycle.

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FIG.2

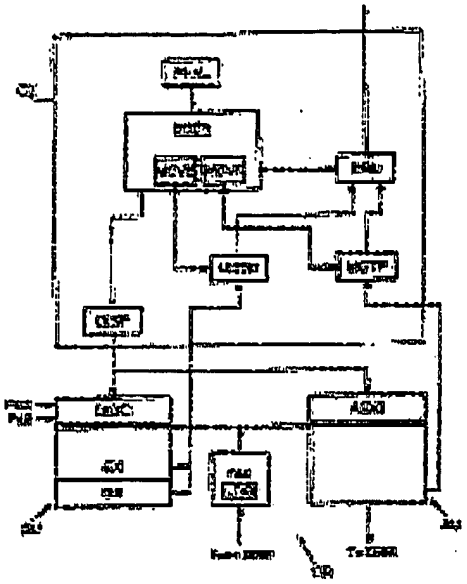

FIG. 2 of the Present Application.

(6) Grounds of Rejection to be Reviewed On Appeal

Claims 25-27, 36-40 and 50 stand rejected under 35 U.S.C. §102(b) as being anticipated by Emma et al. (U.S. Patent No. 5,353,421); and Claim 30 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Emma et al. in combination with European Published Patent Application No. 1050805.

(7) Argument

For the purposes of addressing the rejections, the grouping of the claims is: Claims 25-27 stand together as a group; Claims 36 and 37 stand together as a group and separately from the other groups for the reasons provided below; and Claims

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38-40 and 50 stand together as a group and separately from the other groups for the reasons provided below.

A) The Rejection of independent Claim 38 under 35 USC §102 over Emma et al.

Claim 38 was rejected as being anticipated by Emma et al. (U.S. 5,353,421) for the reasons set forth on pages 4-5 of the Final Office Action. Appellants contend that Claim 38 clearly defines over the cited reference, and in view of the following remarks, reversal of the rejection under 35 U.S.C. §102(b) is requested.

As discussed above, independent Claim 38 is directed to a processor having a central unit for issuing instructions to the processing units based upon corresponding program instructions. The central unit includes a branching module for receiving a branching instruction during a current clock cycle, and processing this branching instruction during the current clock cycle. It is this combination of features which is not fairly taught or suggested in the cited reference and which patentably defines over the cited reference.

The Examiner has relied on the Emma et al. patent as allegedly disclosing a pipelined architecture that "will process a branching instruction immediately without wait when the instruction is received" while referring to Fig. 1 of the Emma et al. patent. Furthermore, the Examiner asserts that the system of Emma et al. includes a central unit for issuing instructions to the processing units based upon corresponding program instructions, and asserts that the central unit includes a branching module for receiving a branching instruction during a current clock cycle, and processing this branching instruction

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during the current clock cycle. The Examiner refers to Figs. 10 and 12 of Emma et al. (reproduced below), and instruction buffer 11 to support his position.

FIG. 10

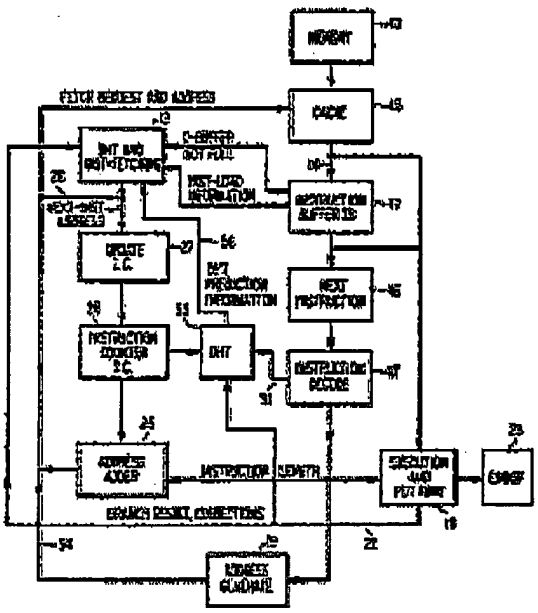
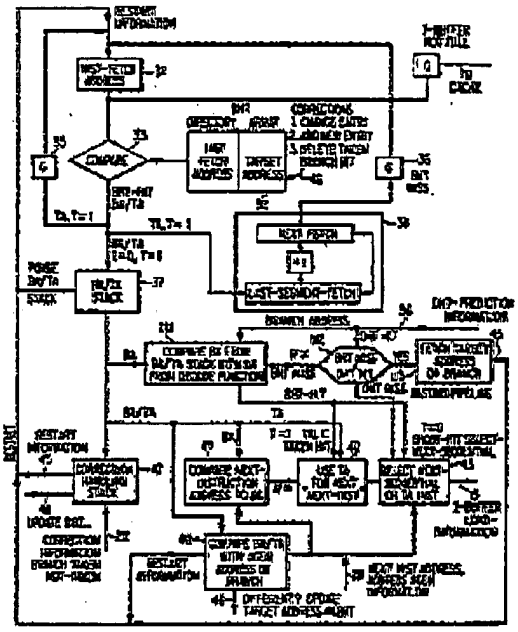


FIG. 12



The Emma et al. patent is directed to a multi-prediction branch prediction mechanism that predicts each conditional branch at least twice, first during the instruction-fetch phase of the pipeline and then again during the decode phase of the pipeline. The mechanism uses at least two different branch prediction mechanisms. The reference discusses "cycles" of the pipeline (e.g. column 1 and column 7) and specifically teaches, at column 5, lines 29-32, that "the BHT makes its prediction during the instruction-fetch phase of the pipeline and

that it can be several cycles until the branch instructions is finally executed."

However, the Examiner has mischaracterized the actual teachings of the Emma et al. reference. Although the instruction buffer 11 (FIG. 10 above) may be considered to be a branching module for receiving a branching instruction, there no suggestion that a branching instruction, received by a central unit in the course of a current clock cycle, is processed during the current clock cycle, as claimed. Indeed, the reference mentions "cycles" and "phases" but provides no teaching whatsoever (see FIGs. 10 and 12, relied upon by the Examiner, above) that a branching module receives a branching instruction during a current clock cycle, and processes this branching instruction during the current clock cycle.

As the Examiner is aware, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim.

There is simply no teaching or suggestion in the cited reference to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Appellants maintain that the cited reference does not disclose or fairly suggest the invention as set forth in Claim 38. Thus, the rejection of Claim 38 under 35 U.S.C. §102(b) should be reversed.

B) The Rejection of independent Claim 36 under 35 USC §102 over Emma et al.

Claim 36 was rejected as being anticipated by Emma et al. for the reasons set forth on pages 3-4 of the Final Office

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Action. Appellants contend that Claim 36 clearly defines over the cited reference, and in view of the following remarks, reversal of the rejection under 35 U.S.C. §102(b) is requested.

As discussed above, independent Claim 36 is directed to a method of handling branching instructions using a processor comprising a program memory storing program instructions, and a processor core comprising a plurality of processing units and a central unit connected thereto, the central unit issuing instructions to the processing units based upon the program instructions. The method includes receiving at the central unit a branching instruction during a current clock cycle and processing the received branching instruction during the current clock cycle. It is this combination of features which is not fairly taught or suggested in the cited reference and which patentably defines over the cited reference.

The Examiner has relied on the Emma et al. patent as allegedly disclosing a pipelined architecture that "will process a branching instruction immediately without wait when the instruction is received" while referring to Fig. 1 of the Emma et al. patent. Furthermore, the Examiner asserts that the method of Emma et al. teaches that the central unit receives a branching instruction during a current clock cycle, and processes this branching instruction during the current clock cycle. The Examiner again referred to Fig. 12 of Emma et al.

As discussed above, there no teaching or suggestion in the Emma et al. reference that a branching instruction, received by a central unit in the course of a current clock cycle, is processed during the current clock cycle, as claimed. Again, Appellants point out that the reference actually discusses "cycles" and "phases" but provides no teaching whatsoever (see

FIG. 12, relied upon by the Examiner, above) that a central unit receives a branching instruction during a current clock cycle, and processes this branching instruction during the current clock cycle.

Again, Appellants note that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim.

There is simply no teaching or suggestion in the cited reference to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Appellants maintain that the cited reference does not disclose or fairly suggest the invention as set forth in Claim 36. Thus, the rejection of Claim 36 under 35 U.S.C. §102(b) should be reversed.

C) The Rejection of independent Claim 25 under 35 USC §102 over Emma et al.

Claim 25 was rejected as being anticipated by Emma et al. for the reasons set forth on pages 2-3 of the Final Office Action. Appellants contend that Claim 25 clearly defines over the cited reference, and in view of the following remarks, reversal of the rejection under 35 U.S.C. §102(b) is requested.

As discussed above, independent Claim 25 is directed to a method of handling branching instructions using a processor comprising a program memory storing program instructions, and a processor core comprising a plurality of processing units and a central unit connected thereto, the central unit issuing instructions to the processing units based upon the program instructions. The method includes clocking the processor core

with a clock signal, receiving a branching instruction in the course of a current cycle, and processing the received branching instruction in the course of the current cycle. It is this combination of features which is not fairly taught or suggested in the cited reference and which patentably defines over the cited reference.

With respect to Claim 25, the Examiner also has relied on the Emma et al. patent as allegedly disclosing a pipelined architecture that "will process a branching instruction immediately without wait when the instruction is received" while referring to Fig. 1 of the Emma et al. patent. Furthermore, the Examiner asserts that the method of Emma et al. teaches that the processor core is clocked with a clock signal and that a branching instruction is received during a current cycle, and processed during the current cycle. The Examiner again referred to Fig. 12 of Emma et al.

As already discussed, there no teaching or suggestion in the Emma et al. reference that a branching instruction, received in the course of a current cycle, is processed during the current cycle, as claimed. Again, Appellants point out that the reference is actually concerned with reducing delay and even discusses "cycles" and "phases." However, Appellants emphasize that nothing in these teachings provides for a branching instruction to be received and processed during a current cycle.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. There is simply no teaching or suggestion in the cited reference to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Appellants maintain that the

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cited reference does not disclose or fairly suggest the invention as set forth in Claim 25. Thus, the rejection of Claim 25 under 35 U.S.C. §102(b) should be reversed.

CONCLUSIONS

In view of the foregoing arguments, it is submitted that all of the claims are patentable over the prior art. Accordingly, the Board of Patent Appeals and Interferences is respectfully requested to reverse the earlier unfavorable decision by the Examiner.

Respectfully submitted,

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APPENDIX A - CLAIMS ON APPEAL
FOR U.S. PATENT APPLICATION SERIAL NO. 10/082,816

25. (Previously presented) A method of handling branching instructions using a processor comprising a program memory storing program instructions, and a processor core comprising a plurality of processing units and a central unit connected thereto, the central unit issuing instructions to the processing units based upon the program instructions, the method comprising:

clocking the processor core with a clock signal;

receiving a branching instruction in the course of a current cycle; and

processing the received branching instruction in the course of the current cycle.

26. (Previously presented) A method according to Claim 25 wherein the processing units comprise a first processing unit including at least one address-pointing register; wherein a branching instruction uses the content of the at least one address-pointing register; and further comprising checking validity of the content of the at least one address-pointing register at the start of the current cycle so that the branching instruction is actually received by the central unit and processed if the content is declared valid, and, in an opposite case, the branching instruction is kept on hold for processing until the content is declared valid.

27. (Previously presented) A method according to Claim 26 further comprising recopying the content of the at least one

address-pointing register into at least one corresponding duplicated address-pointing register; and wherein the checking is of the at least one corresponding duplicated address-pointing register.

30. (Previously presented) A method according to Claim 25 wherein the at least one processing unit comprises a second processing unit including a guard-indication register; wherein in the presence of a guarded branching instruction, a check on validity of the guard indication assigned to the branching instruction and contained in the guard-indication register is carried out at a start of the current cycle; and wherein the guarded branching instruction is actually received by the central unit and processed, if the value of the corresponding guard indication is declared valid, and, in the opposite case, this guarded branching instruction is kept on hold for processing until the value of the corresponding guard indication is declared valid.

36. (Previously presented) A method of handling branching instructions using a processor comprising a program memory storing program instructions, and a processor core comprising a plurality of processing units and a central unit connected thereto, the central unit issuing instructions to the processing units based upon the program instructions, the method comprising:

receiving at the central core a branching instruction during a current clock cycle and processing the received branching instruction during the current clock cycle.

37. (Previously presented) A method according to Claim 36 wherein the processing units comprise a first processing unit including at least one address-pointing register; wherein a branching instruction uses the content of the at least one address-pointing registers; and further comprising checking validity of the content of the at least one address-pointing register at the start of the current clock cycle so that the branching instruction is actually received by the central unit and processed if the content is declared valid, and, in an opposite case, the branching instruction is kept on hold for processing until the content is declared valid.

38. (Previously presented) A processor comprising:

a program memory for storing program instructions; and

a processor core being clocked by a clock signal and comprising a plurality of processing units and a central unit connected thereto, said central unit for issuing instructions to said processing units based upon corresponding program instructions;

said central unit comprising a branching module for receiving a branching instruction during a current clock cycle, and processing this branching instruction during the current clock cycle.

39. (Previously presented) A processor according to Claim 38 wherein a first processing unit includes at least one address pointing register; wherein a branching instruction uses the content of at least one of the address-pointing registers; wherein the central unit includes first validity-checking means able, at the start of the current cycle, to carry out a check on

validity of the content of the at least one pointing register; and wherein the branching instruction is received by the central unit and processed if the content is declared valid, and, in an opposite case, the branching instruction is kept on hold in the program memory until the content is declared valid.

40. (Previously presented) A processor according to Claim 39 wherein said central unit comprises, for each address-pointing register, a duplicated address-pointing register a content of which is a copy of the corresponding address-pointing register; and wherein said first validity-checking means checks validity of the contents of the corresponding duplicated address-pointing register.

50. (Previously presented) A processor according to Claim 38 having a decoupled architecture.

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